This listing of claims will replace all prior versions of claims in the application:

1. (Original) A phase detector circuit that receives a random NRZ signal Vi(t) having a period of T and a signal Vi(t-θT/2π) having the same period and pattern as those of the signal Vi(t) and delayed from the signal Vi(t) by θ in phase, and outputs a signal including a DC voltage component associated with a phase difference θ between said two signals,

wherein an output Vo(t) of the phase detector circuit is represented by:

$$Vo(t)=(Vi(t)-Vi(t-T))xVi(t-\theta T/2\pi),$$

where the signal Vi(t-T) is delayed from the signal Vi(t) by the period T of the signal Vi(t).

2. (Original) A phase detector circuit that outputs a signal including a DC voltage component associated with a phase difference between two input signals, comprising:

a delay circuit for outputting a signal delayed by the time of T, which is a period of an input random NRZ signal;

a subtracter circuit for outputting a difference between said input random NRZ signal and the signal delayed by said delay circuit; and

a multiplier circuit for outputting a product of another input random NRZ signal having the same pattern as that of said input random NRZ signal and said phase difference and an output of said subtracter circuit.

3-5 (Cancelled)

6. (Previously presented) A phase detector circuit that outputs a signal including a DC voltage component associated with a phase difference between two input signals, comprising:

a delay circuit for outputting a signal delayed by the time of (T-δT), which is shorter than the period T of an input random NRZ signal;

a subtracter circuit for outputting a difference between said input random NRZ signal and the signal delayed by said delay circuit;

a multiplier circuit for outputting a product of another input random NRZ signal having the same pattern as that of said input random NRZ signal and said phase difference and an output of said subtracter circuit.

7. (Currently amended) A phase detector circuit that receives a random NRZ signal Vi(t) having a period of T and a signal Vi(t-θT/2π) having the same period and pattern as those of the signal Vi(t) and delayed from the signal Vi(t) by θ in phase, and outputs a signal including a DC voltage component associated with a phase difference θ between said two signals,

wherein an output Vo(t) of the phase detector circuit is represented by:

Vo(t)=(Vi(t)-Vi(t-(~~T-θT~~ T-δT)))xVi(t-θT/2π),

where the signal Vi(t-(T-δT)) is delayed from the signal Vi(t) by the time of (T-δT), which is shorter than the period T of the signal Vi(t).

8. (Currently amended) A phase detector circuit that outputs a DC voltage signal associated with a phase difference between an input random NRZ signal and a second signal related to said input random NRZ signal, comprising:

a delay circuit for delaying said input random NRZ signal by an amount related to a period T of said input random NRZ signal and outputting a delayed signal; and

a combination of at least one multiplier circuit and a ~~subtractor~~ subtracter circuit, which combination performs an arithmetic operation on only said input random NRZ signal, said delayed signal, and said second signal to produce an output signal having a DC voltage component corresponding to said phase difference.

9. (Previously presented) The phase detector circuit of claim 8, wherein said second signal is the same as said input random NRZ signal but differing in phase therefrom by an angle θ, and said delay circuit delays said input random NRZ signal by a value of T.

10. (Previously presented) The phase detector circuit of claim 8, wherein said second signal is the same as said input random NRZ signal but differing in phase therefrom by an angle θ, and said delay circuit delays said input random NRZ signal by a value of $(T-\delta T)$, where δT is a value less than T.

11. (Cancelled)

12. (Previously presented) The phase detector circuit of claim 8, wherein said delay circuit comprises a first voltage-controlled delay circuit and a control circuit for controlling said voltage-controlled delay circuit.

13. (Cancelled)

14. (Currently amended) The phase detector circuit of claim 9, wherein said combination comprises a first multiplier circuit for multiplying said input random NRZ signal with said second signal, a second multiplier circuit for multiplying said second signal with the output of said delay circuit, and said ~~subtractor~~ subtracter circuit subtracts the output of said second multiplier circuit from the output of said first multiplier circuit.

15. (Cancelled)